2nd Generation

DESCRIPTION

This family is a 64M bit dynamic RAM organized 16,777,216 x 4-bit configuration with Extended Data Out mode CMOS DRAMs. Extended data out mode is a kind of page mode which is useful for the read operation. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50 or 60ns) and refresh cycle(8K ref. or 4K ref.)and package(SOJ or TSOP-II) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Extended data out operation
- Read-modify-write capability
- Multi-bit parallel test capability
- LVTTL(3.3V) compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- JEDEC standard pinout
  32-pin plastic SOJ/TSOP-II (400mil)
- Single power supply of 3.3 ± 0.3V
- Early write or output enable controlled write

- Max. Active power dissipation

Speed	8K refresh	4K refresh
50	396mW	504mW
60	324mW	432mW

- Fast access time and cycle time

Speed	tRAC	tCAC	tHPC
50	50ns	13ns	20ns
60	60ns	15ns	25ns

- Refresh cycle

Part number	Refresh	Normal	L-part
HY51V64404A[1)]	8K	64ms	128ms
HY51V65404A[2)]	4K		

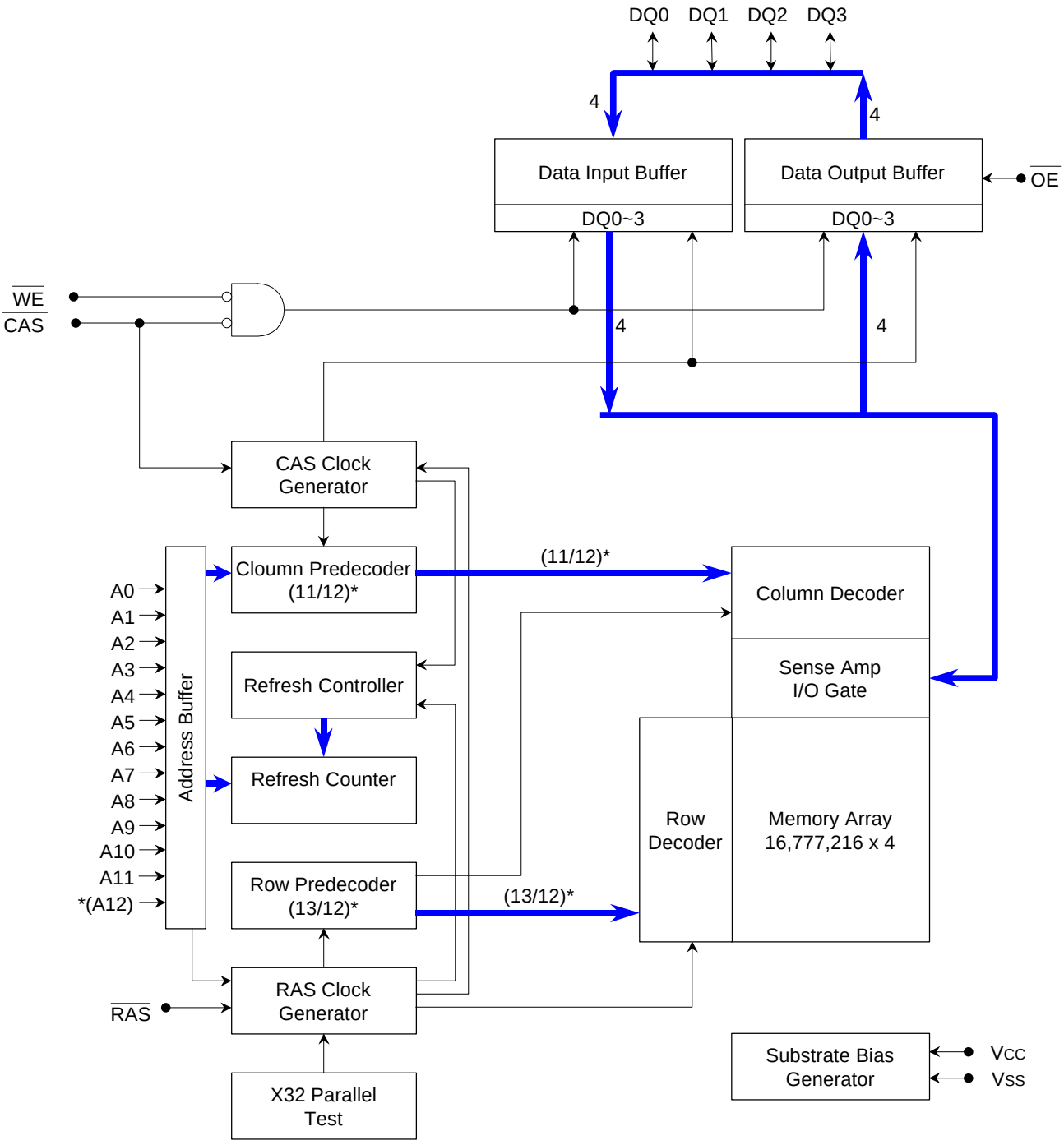
1) Normal read / write, /RAS only refresh : 8K cycles / 64ms
   /CAS-before-/RAS, Hidden refresh : 4K cycles / 64ms
2) Normal read / write, /RAS only refresh : 4K cycles / 64ms
   /CAS-before-/RAS, Hidden refresh : 4K cycles / 64ms

ORDERING INFORMATION

Part Name	Refresh	Power	Package
HY51V64404ATC	8K		32Pin SOJ/TSOP-II
HY51V64404ALTC	8K	L-part	32Pin SOJ/TSOP-II
HY51V64404ASLTC	8K	*SL-part	32Pin SOJ/TSOP-II
HY51V65404ATC	4K		32Pin SOJ/TSOP-II
HY51V65404ALTC	4K	L-part	32Pin SOJ/TSOP-II
HY51V65404ASLTC	4K	*SL-part	32Pin SOJ/TSOP-II

*SL : Self refresh with low power.

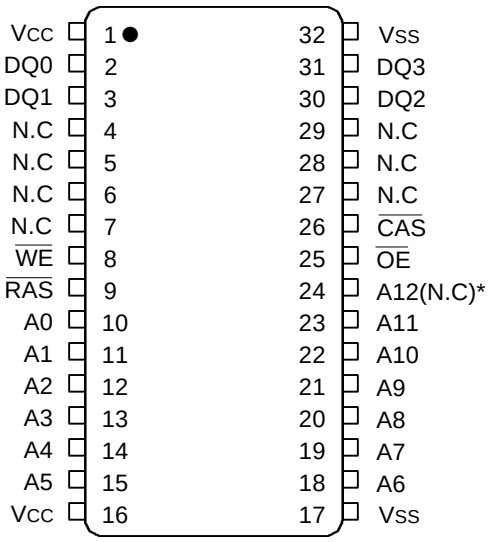
FUNCTIONAL BLOCK DIAGRAM



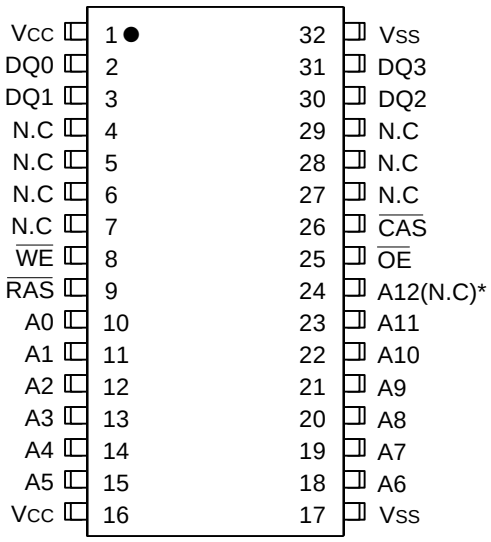
*(A12) for 8K refresh part

(8K Refresh / 4K Refresh)*

PIN CONFIGURATION (Marking Side)



32Pin Plastic SOJ (400mil)



32Pin Plastic TSOP-II (400mil)

A12(N.C)* : For 4K refresh product

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A12	Address Input (8K Refresh Product)
A0~A11	Address Input (4K Refresh Product)
DQ0~DQ3	Data In/Out
Vcc	Power (3.3V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-0.5 to 6.0	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note : Operation at or above Absolute Maximum Ratings could adversely affect device reliability and cause permanent damage.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3[1)]	V
V_{IL}	Input Low Voltage	-0.3[2)]	-	0.8	V

Note : All voltages are referenced to V_{SS}.

1) 6.0V at pulse width 10ns which is measured at V_{CC}.

2) -1.0V at pulse width 10ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test condition	Min	Max	Unit
I_{LI}	Input Leakage Current (Any input)	$V_{SS} \le V_{IN} \le V_{CC}$ + 0.3 All other pins not under test = V_{SS}	-5	5	µA
I_{LO}	Output Leakage Current (Any input)	$V_{SS} \le V_{OUT} \le V_{CC}$ /RAS&/CAS at V_{IH}	-5	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0mA	2.4	-	V

DC CHARACTERISTICS

(T_A = 0°C to 70°C , V_{CC} = 3.3 ± 0.3V , V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max. Current		Unit
				8K refresh	4K refresh	
I_{CC1}	Operating Current	/RAS, /CAS Cycling t_{RC} = $t_{RC(min.)}$	50 60	110 90	140 120	mA
I_{CC2}	LVTTL Standby Current	/RAS, /CAS ≥ V_{IH} Other inputs ≥ V_{SS}		1	1	mA
I_{CC3}	/RAS-only Refresh Current	/RAS Cycling,/CAS = V_{IH} t_{RC} = $t_{RC(min.)}$	50 60	110 90	140 120	mA
I_{CC4}	EDO mode Current	/CAS Cycling, /RAS = V_{IL} t_{HPC} = $t_{HPC(min.)}$	50 60	120 100	130 110	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V_{CC} - 0.2V	L-part	500 300	500 300	µA
I_{CC6}	/CAS-before-/RAS Refresh Current	t_{RC} = $t_{RC(min.)}$	50 60	140 120	140 120	mA
I_{CC7}	Battery Back-up Current (L-part)	V_{IH} = V_{CC} - 0.2V, V_{IL} = 0.2V /CAS = CBR cycling or 0.2V /OE&/WE = V_{IH} = V_{CC} - 0.2V Address = Don't care DQ0~DQ3 = Open, tRAS ≤ 300ns tRC=31.25uS		550	550	µA
I_{CC8}	Self Refresh Current (L-part)	/RAS&/CAS = 0.2V Other pins are same as I_{CC7}		450	450	µA

Note

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(t_{RC} and t_{HPC}).
2. Specified values are obtained with output unloaded.
3. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, address can be changed only once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /CAS=V_{IH} withen one EDO mode cycle time t_{HPC}.

AC CHARACTERISTICS

(T_A = 0 °C to 70 °C, V_{CC} = 3.3 ± 0.3V , V_{SS} = 0V, unless otherwise noted.)

#	Symbol	Parameter	50ns		60ns		Unit	Note
			Min	Max	Min	Max		
1	t_{RC}	Random read or write cycle time	84	-	104	-	ns	
2	t_{RWC}	Read-modify-write cycle time	120	-	140	-	ns	
3	t_{HPC}	EDO mode cycle time	20	-	25	-	ns	
4	t_{HPRWC}	EDO mode read-modify-write cycle time	57	-	65	-	ns	
5	t_{RAC}	Access time from /RAS	-	50	-	60	ns	4,5,10,11
6	t_{CAC}	Access time from /CAS	-	13	-	15	ns	4,5,10
7	t_{AA}	Access time from column address	-	25	-	30	ns	4,5,11
8	t_{CPA}	Access time from /CAS precharge	-	30	-	35	ns	4
9	t_{CLZ}	/CAS to output low impedance	0	-	0	-	ns	3
10	t_{CEZ}	Output buffer turn-off delay from /CAS	0	10	0	15	ns	
11	t_{OLZ}	/OE to output in low impedance	0	-	0	-	ns	
12	t_T	Transition time(rise and fall)	2	50	2	50	ns	4
13	t_{RP}	/RAS precharge time	30	-	40	-	ns	
14	t_{RAS}	/RAS pulse width	50	10K	60	10K	ns	
15	t_{RASP}	/RAS pulse width(EDO mode)	50	100K	60	100K	ns	
16	t_{RSH}	/RAS hold time	13	-	15	-	ns	
17	t_{CSH}	/CAS hold time	40	-	45	-	ns	
18	t_{CAS}	/CAS pulse width	8	10K	10	10K	ns	
19	t_{RCD}	/RAS to /CAS delay time	15	37	20	45	ns	10
20	t_{RAD}	/RAS to column address delay time	13	25	15	30	ns	11
21	t_{CRP}	/CAS to /RAS precharge time	5	-	5	-	ns	
22	t_{CP}	/CAS precharge time	8	-	10	-	ns	15
23	t_{ASR}	Row address set-up time	0	-	0	-	ns	
24	t_{RAH}	Row address hold time	8	-	10	-	ns	
25	t_{ASC}	Column address set-up time	0	-	0	-	ns	14
26	t_{CAH}	Column address hold time	8	-	10	-	ns	14
27	t_{RAL}	Column address to /RAS lead time	25	-	30	-	ns	
28	t_{RCS}	Read command set-up time	0	-	0	-	ns	
29	t_{RCH}	Read command hold time referenced to /CAS	0	-	0	-	ns	7
30	t_{RRH}	Read command hold time referenced to /RAS	0	-	0	-	ns	7
31	t_{WCH}	Write command hold time	10	-	10	-	ns	

AC CHARACTERISTICS

Continued

#	Symbol	Parameter	50ns		60ns		Unit	Note
			Min	Max	Min	Max		
32	tWP	Write command pulse width	8	-	10	-	ns	
33	tRWL	Write command to /RAS lead time	15	-	15	-	ns	
34	tCWL	Write command to /CAS lead time	8	-	10	-	ns	17
35	tDS	Data-in set-up time	0	-	0	-	ns	8,20
36	tDH	Data-in hold time	10	-	10	-	ns	8,20
37	tREF	Refresh period(4096 cycles)	-	64	-	64	ms	12,13
		Refresh period(8192 cycles)	-	64	-	64	ms	12,13
		Refresh period(L-part)	-	128	-	128	ms	12,13
38	tWCS	Write command set-up time	0	-	0	-	ns	9
39	tCWD	/CAS to /WE delay time	34	-	36	-	ns	9,16
40	tRWD	/RAS to /WE delay time	70	-	80	-	ns	9
41	tAWD	Column address to /WE delay time	45	-	50	-	ns	9
42	tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	ns	18
43	tCHR	/CAS hold time(CBR cycle)	10	-	10	-	ns	19
44	tRPC	/RAS to /CAS precharge time	5	-	5	-	ns	
45	tCPT	/CAS precharge time(CBR counter test)	25	-	30	-	ns	
46	tROH	/RAS hold time referenced to /OE	5	-	5	-	ns	
47	tOEA	/OE access time	-	13	-	15	ns	
48	tOED	/OE to data delay	13	-	15	-	ns	
49	tOEZ	Output buffer turn-off delay time from /OE	0	10	0	15	ns	6
50	tOEH	/OE command hold time	13	-	15	-	ns	
51	tCPWD	/WE delay time from /CAS precharge	45	-	54	-	ns	6
52	tRHCP	/RAS hold time from /CAS precharge	30	-	35	-	ns	
53	tWRP	/WE to /RAS precharge time(CBR cycle)	10	-	10	-	ns	
54	tWRH	/WE to /RAS hold time(CBR cycle)	10	-	10	-	ns	
55	tWTS	Write command set-up time(test mode in)	10	-	10	-	ns	
56	tWTH	Write command hold time(test mode in)	10	-	10	-	ns	
57	tRASS	/RAS pulse width(self refresh)	100K	-	100K	-	ns	

AC CHARACTERISTICS

Continued

#	Symbol	Parameter	50ns		60ns		Unit	Note
			Min	Max	Min	Max		
58	tRPS	/RAS precharge time(self refresh)	100	-	110	-	ns	
59	tCHS	/CAS hold time(self refresh)	-50	-	-50	-	ns	
60	tDOH	Output data hold time	5	-	5	-	ns	
61	tREZ	Output buffer turn-off delay from /RAS	0	10	0	15	ns	6
62	tWEZ	Output buffer turn-off delay from /WE	0	10	0	15	ns	6
63	tWED	/WE to data delay time	15	-	15	-	ns	
64	tOEP	/OE precharge time	5	-	5	-	ns	
65	tWPE	/WE pulse width(EDO cycle)	5	-	5	-	ns	
66	tOCH	/OE to /CAS hold time	5	-	5	-	ns	
67	tCHO	/CAS hold time to /OE	5	-	5	-	ns	

TEST MODE

#	Symbol	Parameter	50ns		60ns		Unit	Note
			Min	Max	Min	Max		
1	tRC	Random read or write cycle time	89	-	109	-	ns	
2	tRWC	Read-modify-write cycle time	125	-	145	-	ns	
3	tHPC	EDO mode cycle time	25	-	30	-	ns	
4	tHPRWC	EDO mode read-modify-write cycle time	62	-	70	-	ns	
5	tRAC	Access time from /RAS	-	55	-	65	ns	4,5,10,11
6	tCAC	Access time from /CAS	-	18	-	20	ns	4,5,10
7	tAA	Access time from column address	-	30	-	35	ns	4,5,11
8	tCPA	Access time from /CAS precharge	-	35	-	40	ns	4
14	tRAS	/RAS pulse width	55	10K	65	10K	ns	
15	tRASP	/RAS pulse width(EDO mode)	55	100K	65	100K	ns	
16	tRSH	/RAS hold time	18	-	20	-	ns	4
17	tCSH	/CAS hold time	45	-	55	-	ns	
18	tCAS	/CAS pulse width	13	10K	15	10K	ns	
27	tRAL	Column address to /RAS lead time	30	-	35	-	ns	
39	tCWD	/CAS to /WE delay time	39	-	41	-	ns	16
40	tRWD	/RAS to /WE delay time	75	-	85	-	ns	
41	tAWD	Column address to /WE delay time	50	-	55	-	ns	9
47	tOEA	/OE access time	-	18	-	20	ns	
48	tOED	/OE to data delay	18	-	20	-	ns	
50	tOEH	/OE command hold time	18	-	20	-	ns	
51	tCPWD	/WE delay time from /CAS precharge	50	-	59	-	ns	9

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS-only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS- before-/RAS initialization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit parallel test mode during initialization.
2. If /RAS=V_{SS} during power-up, the HY51V64404A, HY51V65404A could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up.
3. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
4. $V_{IH(min.)}$ and $V_{IL(max.)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min.)}$ and $V_{IL(max.)}$, and are assumed to be 2ns for all inputs.
5. Measured at V_{OH}=2.0V and VOL=0.8V with a load equivalent to 1TTL loads and 100pF.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in read-modify-write cycles and late write cycle.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD(min.)}$, $t_{CWD} \geq t_{CWD(min.)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPWD} \geq t_{CPWD(min.)}$, the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the $t_{RCD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA}.
11. $t_{REF(max)}$=128ms is applied to L-parts .
12. A burst of 4096(4k refresh part) /RAS-only refresh cycles must be executed within 64ms (128ms for L-parts) after exiting self refresh.A burst of 8192(8k refresh part) /RAS-only refresh cycles must be executed within 64ms (128ms for L-parts) after exiting self refresh.(CBR refresh & Hidden refresh : 4K cycle/64ms)
13. t_{ASC},t_{CAH} are referenced to the earlier /CAS falling edge.

CAPACITANCE

(T_A = 0°C to 70°C , V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, f = 1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Input Capacitance (A0~A12)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input / Output Capacitance (DQ0~DQ7)	-	7	pF